Siliconix incorporated

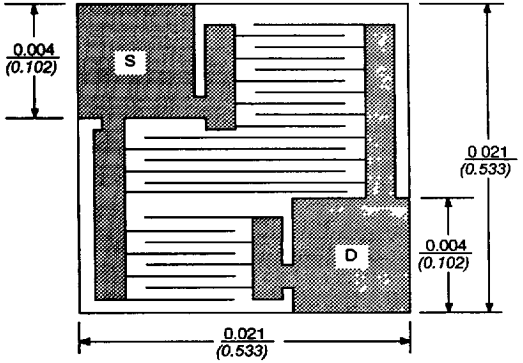
PSCIA SERIES DIE
P-Channel JFETs

T-37-25

The PSCIA Series is a p-channel JFET analog switch designed to complement our n-channel NCB Series. They feature low on-resistance and good off-isolation as well as the fast switching associated with JFETs. Die are supplied with 100% visual sort to the criteria of MIL-STD-750C, Method 2072.

PSCIA1CHP*	PSCIA2CHP*	PSCIA3CHP*	PSCIA4CHP*
2N5114 J174 SST174	2N5115 J175 SST175	2N5116 J176 SST176	J177 SST177
*Meets or exceeds specification for all part numbers listed below			

For additional design information please consult the typical performance curves PSCIA.



Gate backside contact

Nominal Thickness
0.009 inches
0.228 mm

DESIGNED FOR:

- Analog Switches
- Commutators
- Choppers
- Integrator Reset Switch

FEATURES

- Low Insertion Loss in Switching Systems
  $r_{DS(ON)} < 75\ \Omega$ (2N5114)
- Short Sample and Hold Aperture Time
  $C_{rss} < 7$ pF
- High Off-Isolation $I_{D(OFF)} < 500$ pA

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ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Gate-Drain Voltage	V_{GD}	30	V
Gate-Source Voltage	V_{GS}	30	
Gate Current	I_G	50	mA
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to 150	°C

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SPECIFICATIONS[a]				LIMITS					
					PSCIA1CHP		PSCIA2CHP		
PARAMETER	SYMBOL	TEST CONDITIONS		TYP[b]	MIN	MAX	MIN	MAX	UNIT
STATIC									
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = 1 µA, V_{DS} = 0 V		45	30		30		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = −15 V, I_D = −1 nA			5	10	3	6	
Saturation Drain Current[c]	I_{DSS}	V_{GS} = 0 V	V_{DS} = −18 V		−30	−90			mA
			V_{DS} = −15 V				−15	−60	
Gate Reverse Current	I_{GSS}	V_{GS} = −20 V, V_{DS} = 0 V		5					pA
			T_A = 150°C	0.01					µA
Gate Operating Current	I_G	V_{DG} = −15 V, I_D = −1 mA		−5					pA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = −15 V, V_{GS} > $V_{GS(OFF)}$		−10					
			T_A = 150°C	−0.02					nA
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, I_D = −1 mA				75		100	Ω
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = −1 mA, V_{DS} = 0 V		−0.7					V
DYNAMIC									
Common-Source Forward Transconductance	g_{fs}	V_{DG} = −15 V, I_D = −1 mA f = 1 kHz		4.5					mS
Common-Source Output Conductance	g_{os}			20					µS
Drain-Source On-Resistance	$r_{ds(ON)}$	V_{GS} = 0 V, I_D = 0 V, f = 1 kHz				75		100	Ω
Common-Source Input Capacitance	C_{iss}	V_{DS} = −15 V, V_{GS} = 0 V f = 1 MHz		20					pF
Common-Source Reverse Transfer Capacitance	C_{rss}	V_{DS} = 0 V, V_{GS} > $V_{GS(OFF)}$ f = 1 MHz		5					
Equivalent Input Noise Voltage	$\overline{e}_n$	V_{DG} = −10 V, I_D = −1 mA f = 1 kHz		20					$nV/\sqrt{Hz}$
SWITCHING									
Turn-On Time	$t_{d(ON)}$	$V_{GS(ON)}$ = 0 V		6					ns
	t_r	P/N V_{DD} $I_{D(ON)}$ $V_{GS(OFF)}$ R_L		10					
Turn-Off Time	$t_{d(OFF)}$	PSCIA1 −10V −15mA 20V 130Ω PSCIA2 −6V −7mA 12V 900Ω		6					
	t_f			15					

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = 300 µS, duty cycle ≤ 2%.

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PSCIA SERIES DIE

SPECIFICATIONS[a]			LIMITS					
				PSCIA3CHP		PSCIA4CHP		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	MIN	MAX	UNIT
STATIC								
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = 1 µA, V_{DS} = 0 V	45	30		30		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = −15 V, I_D = −10 nA		1	4	0.3	2.25	
Saturation Drain Current[c]	I_{DSS}	V_{GS} = 0 V, V_{DS} = −18 V						mA
		V_{DS} = −15 V		−5	−25	−1.5	−20	
Gate Reverse Current	I_{GSS}	V_{GS} = −20 V, V_{DS} = 0 V	5					pA
		T_A = 150°C	0.01					µA
Gate Operating Current	I_G	V_{DG} = −15 V, I_D = −1 mA	−5					pA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = −15 V, V_{GS} > $V_{GS(OFF)}$	−10					
		T_A = 150°C	−0.02					nA
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, I_D = −1 mA			150		300	Ω
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = −1 mA, V_{DS} = 0 V	−0.7					V
DYNAMIC								
Common-Source Forward Transconductance	g_{fs}	V_{DG} = −15 V, I_D = −1 mA, f = 1 kHz	4.5					mS
Common-Source Output Conductance	g_{os}		20					µS
Drain-Source On-Resistance	$r_{ds(ON)}$	V_{GS} = 0 V, I_D = 0 V, f = 1 kHz			175		300	Ω
Common-Source Input Capacitance	C_{iss}	V_{DS} = −15 V, V_{GS} = 0 V, f = 1 MHz	20					pF
Common-Source Reverse Transfer Capacitance	C_{rss}	V_{DS} = 0 V, V_{GS} > $V_{GS(OFF)}$, f = 1 MHz	5					
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DG} = −10 V, I_D = −1 mA, f = 1 kHz	20					$nV/\sqrt{Hz}$
SWITCHING								
Turn-On Time	$t_{d(ON)}$	$V_{GS(ON)}$ = 0 V	6					ns
	t_r	P/N V_{DD} $I_{D(ON)}$ $V_{GS(OFF)}$ R_L	10					
Turn-Off Time	$t_{d(OFF)}$	PSCIA3 −6V −3mA 8V 2000Ω	6					
	t_f	PSCIA4 −6V −3mA 8V 2000Ω	15					

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = 300 µS, duty cycle ≤ 2%.

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